ESD protection device and circuit design for advanced CMOS technologies

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***Abstract*— The challenges associated with the design and implementation of Electrostatic Discharge (ESD) protection circuits are becoming increasingly complex as technology is scaled well into nano-metric regime. Traditional approaches of ESD design may not be adequate as the ESD damages occur at successively lower voltages in nano-metric dimensions. There are several challenges that must be met in order to design robust ESD circuits today. Due to technology scaling and proliferation of automated handling, ESD failures in ICs caused by Charged Device Model (CDM) are increasing. CDM discharges can cause latent damages which could degrade and eventually lead to definite failures in the ICs. The ESD protection design for current and future sub-65nm CMOS circuits is a challenge for high I/O count, multiple power domains and flip-chip products. In this talk, we will address some of the above mentioned challenges and discuss some of the solutions.**