Design Methodology for ESD Power Supply Clamps in Advanced CMOS Technologies

Mahdi Elghazali, Manoj Sachdev and Ajoy Opal
Dept. of Electrical and Computer Engineering
University of Waterloo, Waterloo, ON, Canada, N2L 3G1
phone: (1) 519-888-4567 ext. 31449
e-mail: melghazali@uwaterloo.ca

***Abstract*—Electrostatic Discharge (ESD) is one of the major reliability issues in advanced CMOS technologies. Research has shown that only I/O based ESD protection circuits are inadequate in providing necessary ESD protection. Therefore, it is important to have an effective ESD power supply clamp across the power supply rails so that the ESD event will be discharged through it and protects the circuit core. In this paper, we propose a design methodology for ESD power supply clamps in advanced CMOS technologies. The design methodology consists of four major steps: technology characterization, designing the circuit, simulation and measurement. Based on simulation and measurement results, the design is modified to improve performance. A static ESD power supply clamp in 65 nm CMOS technology is provided as a study case.**

I. Introduction

One of the well-known reliability issues in integrated circuit industry is Electrostatic Discharge (ESD) that has an impact on the yield and cost of fabrication. Designing efficient ESD protection circuits has become essential to prevent ESD related yield loss [1]. As the ESD event happens, it balances the charge between two objects and leads to high current in very short time. As the current passes through an object, a voltage is developed across it and results in creating an electric field. If one of these objects happens to be a semiconductor device, it is damaged by both the high current density and the high electric field [2]. The high current density damages the semiconductor devices through thin-film fusing, filamentation, and junction spiking [3]. The high electric field, on the other hand, can cause failure through dielectric breakdown or charge injection [3]. ESD protection for an IC is limited by the oxide breakdown ($BVOX_{ESD}$) [4]. Therefore, it is important to design ESD protection circuits that are able to prevent these failures. Often ESD protection targets are desirable for a given technology that ensure low losses due to ESD. It is desired to have an ESD protection circuit that react fast to ESD stress, stays on for the entire ESD stress, is stays stable and has low-leakage current under the normal operating conditions.

Fig. 1 shows the typical chip-level ESD protection scheme in which an ESD power supply clamp is connected between the two power supply rails. The main goal of ESD protection circuits is to provide a low-resistive discharge path from any two pins on the chip. The circuit core is susceptible to ESD damage if there are only ESD protection circuits at the I/O pads. As shown in Fig. 1, the ESD clamp provides the discharge path for an ESD event that happens between the two power rails (PSD-mode, NDS-mode). The clamp is also part of the discharge path for both PS-mode and ND-mode. Thus, it is important to have an effective ESD power supply clamp across the power supply rails [5].

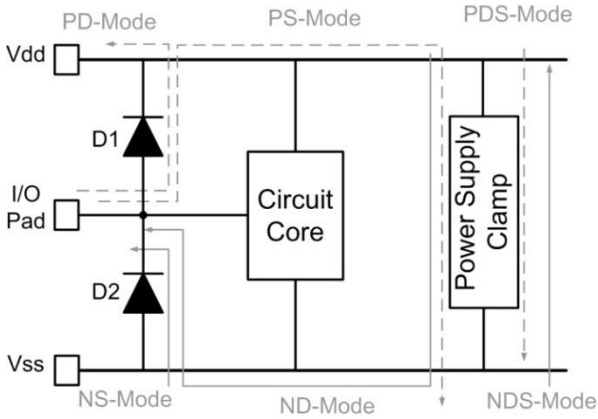

Fig. 1. Typical chip-level ESD protection scheme under different ESD stresses.

Under the normal operating condition of the circuit core, the ESD clamp should have very low-leakage current and should be stable and immune to the power supply noise. In addition, the ESD clamp must effectively react to an ESD event. In recent years, there have been attempts to design different ESD power supply clamps to achieve the characteristics mentioned above. These designs fall under one of two categories: (i) Static clamps and (ii) Transient clamps. The static ESD clamp turns on once the voltage across the supply rails exceeds the triggering voltage and starts conducting the current of the ESD event. Many designs and structures have been proposed such as the string of diodes, Grounded-Gate NMOS transistor, and Zener diode based [5]. The main disadvantage of static clamps is that the clamp does not stay on for a long enough time to safely sink the entire energy associated with an ESD event [5].

The transient ESD clamps take advantage of the rapid change in voltage during an ESD event to trigger the clamp using a rise time detector and a delay element to keep the clamping element on during the entire ESD event. The rise time detector network that consists of a resistance and a capacitance is usually set to 40 ns so that it distinguishes between the normal noisy power supply and the ESD event [6]. Several designs have been proposed based on this concept [6], [7], [8]. Transient clamps are able to react fast; however, these circuits must be carefully designed to keep their leakage to minimum [9]. In this paper, a design methodology for designing ESD power supply clamps is presented. The methodology aims to provide a complete characterization for the designed circuit to ensure excellent protection against ESD events and to reduce the design and test times.

II. The Proposed Design Methodology

Fig. 2 shows the proposed design methodology. The first step is technology characterization, followed by designing the ESD protection circuit to meet the requirement based on the technology characterization and the circuit core to be protected. The third step is to simulate the proposed ESD clamp under both ESD conditions and normal operating condition. The last step is to measure the performance of the proposed ESD protection circuit under both ESD stresses and normal operating conditions.

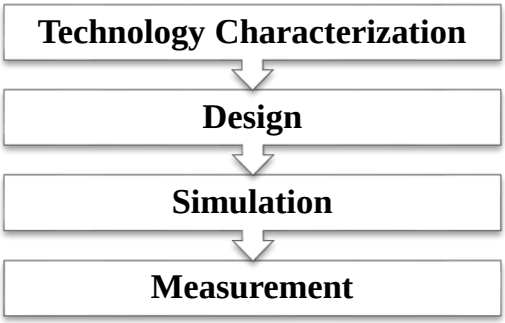

Fig. 2. The proposed design methodology.

A. Technology characterization

The first step in designing an ESD power supply clamp is technology characterization in which several aspects about the technology used and the application must be known. Firstly, the breakdown voltage of the circuit core due to an ESD stress should be known. Secondly, the target ESD protection level should also be known in order to design an ESD protection circuit that limits the voltage across the circuit core below the breakdown voltage. For example, the oxide breakdown voltage for 65 nm CMOS technology is 5 V and the target HBM is 1.5 kV [4]. Therefore, under 1.5 kV HBM stress the voltage between the stressed pins should be less than 5 V to ensure the correct functionality. Thirdly, based on the available components those can be utilized as ESD clamping elements in the technology used and the target application, the design decisions can be taken to tradeoff the ESD performance, the design area, and the leakage current. For instance, silicon controlled rectifier (SCR) has a high current carrying capability; however, it cannot be used in an application where ionizing radiation or hot switching is expected [3].

B. Circuit design

To ensure that the proposed design has the characteristics described in section I, Table 1 presents the specifications that need to be met for the proposed designs. Under normal operating conditions, the ESD clamp should have a very low-leakage current since it is turned off during this mode of operation. In addition, the ESD clamp should be immune to latch-up due to noise on the power supply rails or due to an ESD event. The latch-up represents the case where the clamp turns on due to noise at the power supply rail or stays on after the ESD stress ends. Lastly, the ESD clamp reacts fast to the ESD event and stays on the entire ESD event.

TABLE 1: THE SPECIFICATION TO BE MET FOR THE PROPOSED DESIGN

Design Specifications		Criterion	Reason
Under normal operating conditions	Leakage	Minimum	To minimize the impact of ESD clamp on circuit core
	Latch-up	Immune	
Under ESD stress	V_p (CDM)	$< BVOX_{ESD}$	To protect the circuit core
	On-Time	$>$ 500 ns	To stay on for the entire HBM
	Triggering Voltage (V_t)	$1.2 * V_{DD} < V_t < BVOX_{ESD}$	To protect the circuit core and to avoid latch-up

C. Simulation

The importance of the simulation and the measurement steps is to ensure that the proposed design meets the ESD protection level and does not have a huge impact on the core circuit in terms of leakage and parasitic loading. This section presents the simulations that need to be carried out to have a complete characterization of any ESD power supply clamp in order to ensure the correct functionality and to reduce the number of the required tape-outs. The ESD clamp design can be modified to compromise its performance under both ESD stress and normal operating conditions.

1) ESD simulations

Firstly, the proposed design is simulated under ESD stress using both human body model (HBM) as well as charged device model (CDM). HBM models a charged human body dissipating the ESD event current through grounded IC; the Military Standard (Method 3015.8) [10] can be used. CDM, on the other hand, models the case where the IC itself is charged and being discharged when it touches a grounded element; the JEDEC standard (JESD22-C101C) [11] can be used. The main goal of these two simulations is to ensure that the voltage across the ESD clamp does not exceed the breakdown voltage of the circuit core under the target ESD protection level.

2) Normal operating condition simulations

Under normal operating condition, the ESD protection circuits should not have any impact on the circuit core [5]. The ESD clamp is simulated under the following:

a) Immunity to false triggering:

The first power-on condition can be simulated by applying the normal supply voltage with a 100 ns rise time to V_{DD} node with grounded V_{SS} node. The current through the device and the voltage across it are monitored. The ESD protection circuit should not be triggered due to the first power-on condition.

b) Immunity to power supply noise:

The immunity to power supply noise can be studied by adding a sinusoidal signal with a wide frequency range starting with near DC up to 3 GHz and amplitude of 20% of the normal supply voltage to the power supply node with grounded V_{SS} node. Once again, the current through the ESD structure as well as the voltage across are monitored. The ESD protection circuit should stay off and not be triggered due to a noisy power supply.

c) Leakage current simulation:

The leakage of the clamp is studied at various temperatures. The leakage can be investigated by applying the normal supply voltage to the power supply node of the clamp circuit with grounded V_{SS} node and simulate it over the temperature range of the application. For instance, the industrial standard for the temperature range is -40ºC - 85ºC.

D. Measurements

Once the designer is comfortable with the simulation results, the design can be fabricated and tested under both the ESD stress and normal operating conditions. The measurement can be done at component level (i.e. the ESD protection circuit alone), I/O level (i.e. ESD protection circuit with I/O cell), or at chip level [5]. The focus of this paper is on testing the ESD power supply clamps at the device level.

1) ESD Performance:

a) Turn-on verification:

The turn-on mechanism of the proposed clamps is verified under both the chip not powered and chip powered conditions. The chip not powered condition is carried out to observe the turn-on response of the proposed clamps. The chip powered, on contrary, is carried out to check latch-up issues. In both cases, a positive ESD-like pulse voltage with 20 ns rise time and a width of (100 ns – 500 ns) is applied to V_{DD} node with grounded V_{SS}. Under the chip not powered condition, the voltage before and after applying the pulse should be zero, whereas under the chip powered, the normal operating voltage should be applied before and after applying the pulse**.**

b) Transmission line pulsing (TLP) measurement:

TLP measurement is widely used in the industry to characterize the ESD protection circuits as it offers a reliable, repeatable and nondestructive means for testing ESD circuits. Also, TLP with a pulse width of 100 ns initiates the same junction damage at the same peak current as the HBM stress [5]. A TLP system generates pulses that have 10 ns rise time and a width of 100 ns. The amplitude of the pulses is gradually increased till the clamp fails. After each pulse, the leakage current of the clamp is measured to check if the design has failed or not. A clamp is considered failed when its leakage current increases significantly [12].

c) HBM and CDM measurements:

The proposed clamps should also be subjected to HBM and CDM testing using the Military Standard (Method 3015.8) [10] for HBM measurements and the JESD22-C101F [11] for the CDM measurements. For both measurements, the leakage current is usually traced before and after each zapping and the clamp is considered failed if the leakage current significantly increases after the zapping.

2) Normal operating conditions:

a) Immunity to false triggering:

The first power-on condition can be tested by applying the normal supply voltage with different rise times to V_{DD} node with grounded V_{SS} node. The current through the device and the voltage across it are monitored. The result of the test is to show the rising time

needed to trigger the clamp. The clamp should trigger when the rising time is within the ESD event range (< 20 ns) and does not trigger to events slower than 20 ns.

b) Leakage:

Based on the expected operating temperature, the leakage of the ESD clamp can be investigated by applying the normal supply voltage to the power supply node with grounded V_{SS} node and using a temperature chamber to control the ambient temperature within the operating temperature range.

c) Immunity to transient latch-up:

Transient-induced latch-up (TLU) test is the technique to investigate the vulnerability of an ESD protection device to the transient noise in the power rails under normal operating conditions. The TLU measurement setup at the component-level can precisely simulate the ESD-induced noise on the power rails under system-level ESD test [13]. The test setup described in [13] can be used to investigate the transient latch-up issue.

III. AN EXAMPLE OF ESD CIRCUIT DESIGN

The proposed design methodology was used to design an ESD power supply clamps in 65 nm CMOS technology. In [14], we proposed a static clamp with a thyristor as a delay element to extend the on-time of the clamp under the ESD stress. Fig. 3 shows the schematic of the clamp, while Table 2 presents the design decisions taken to meet the requirements. The main target of this design was to reduce the leakage current of the clamp under normal operating condition without significantly degrading the ESD performance. The thick gate oxide NMOS transistor was used as a clamping element as it has two orders of magnitudes lower leakage than the thin gate oxide transistor with the same dimensions. The measurement results showed that the design is capable of handling 3.21 A of current under ESD stress and it is leakage current is only 180 pA at room temperature. Moreover, the clamp passes +3.5 kV and -4.5 kV HBM stress and +700 and -450 V CDM stress.

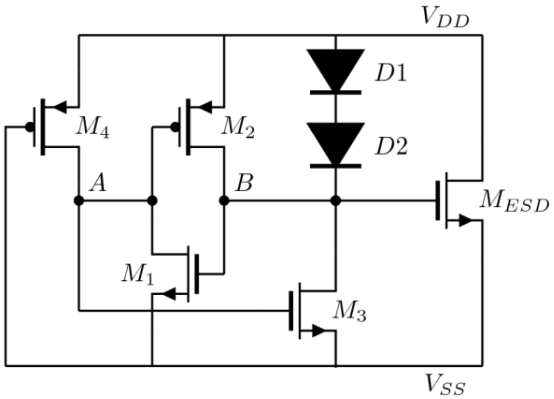

Fig. 3. A static ESD clamp proposed in 65 nm [14].

TABLE 2: THE DECISIONS TO MEET THE DESIGN REQUIREMENTS

Design Requirements		Criterion	Criterion met by
Under normal operating conditions	Leakage	Minimum	Using thick oxide MOS
	Latch-up	Immune	Using guard rings
Under ESD stress	V_p (CDM)	< $BVOX_{ESD}$	Width of M_{ESD} = 2000 µm
	On-Time	> 500 ns	M_1 and M_2 sized to keep M_{ESD} on
	Triggering Voltage (V_t)	1.2 * V_{DD} < V_t < $BVOX_{ESD}$	D_1 and D_2 to trigger M_{ESD}

IV. CHIP LEVEL IMPLEMENTATION CONSIDERATION

In order to have a complete picture, the chip level implementation should be considered. In the typical chip-level ESD protection scheme showing in Fig. 1, assume there is a positive stress at I/O with V_{SS} node is grounded (PS-mode). The discharge path would be through the forward diode (D_1), the two power rails (V_{DD} and V_{SS}) and through the ESD clamp. Therefore, it is important to design the diodes, the powers rails and the clamps to be able to carry the current of the target level ESD stress. The voltage across the two stressed nodes (ΔV_{PS}) is:

$$\Delta V_{PS} = I_{ESD} * \left(R_{on,D_1} + R_{V_{DD}} + R_{on,ESD\ clamp} + R_{V_{SS}}\right) + V_{on,D_1} \quad (1)$$

At the component level, both the clamp and the power-rails resistances where taken into account. At the chip level, the diode on-resistance of the diode and voltage drop across it should be considered. For example, in the 65 nm CMOS technology, the I/O transistors have a gate oxide that is almost three times thicker than the core transistors; therefore, the I/O transistors have a higher breakdown voltage. Thus, designing the clamp at the component level to limit the voltage across it below the breakdown voltage of the core is fine. However, if the I/O transistors have the same breakdown voltage as the core transistors then the whole discharge path should be considered during the design stage.

V. CONCLUSION

One of the well-known reliability issues in the IC industry is ESD that has an impact on the yield and cost of fabrication. To prevent ESD related yield loss, designing efficient ESD protection circuits has become essential. A design methodology for designing ESD power supply clamps in advanced technologies is presented in this paper. The design methodology consists of four major steps: technology characterization, designing the circuit, simulations and measurements. Intensive simulations and measurements will provide a complete characterization of the ESD clamp. In addition, the design methodology covers most of the important aspects to be considered while designing any ESD clamp which will result in reducing the design and test times. The methodology was used to design a static ESD power supply clamp in 65 nm CMOS technology is provided as an example.

REFERENCES

[1] J. B. Huang and G. Wang, "ESD Protection Design for Advanced CMOS," *Proc. of SPIE*, vol. 4600, pp. 123-131, 2001.

[2] J. Vinson and J. Liou, "Electrostatic Discharge in Semiconductor Devices: An Overview," *Proceeding of The IEEE*, vol. 86, no. 2, pp. 399-418, 1998.

[3] J. Vinson and J. Liou, "Electrostatic Discharge in Semiconductor Devices: Protection Techniques," *Proceeding of The IEEE*, vol. 88, no. 12, pp. 1878-1900, 2000.

[4] C. Duvvury, "Paradigm Shift in ESD Qualification," in *IEEE International Reliability Physics Symposium*, 2008.

[5] O. Semenov, H. Sarbishaei and M. Sachdev, ESD Protection Devices and Circuit Design for Advanced CMOS Technologies, Springer science, 2008.

[6] M. Stockinger, J. Miller, M. Khazhinsky, C. Torres, J. Weldon, B. Preble, M. Bayer, M. Akers and V. Kamat, "Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies," in *EOS/ESD Symposium*, 2003.

[7] J. Smith and G. Boselli, "A MOSFET Power Supply Clamp with Feedback Enhanced Triggering for ESD Protection in Advanced CMOS Technologies," in *EOS/ESD Symposium*, 2003.

[8] J. Smith, R. Cline and G. Boselli, "A Low Leakage Low Cost-PMOS Based Power Supply Clamp with Active Feedback for ESD Protection in 65 nm CMOS Technologies," in *EOS/ESD Symposium*, 2005.

[9] M. Ker and C. Yeh, "On the Design of Power-Rail ESD Clamp Circuits With Gate Leakage Consideration in Nanoscale CMOS Technology," *IEEE Transactions on Device and Material Reliability*, vol. 14, no. 1, pp. 536-544, 2014.

[10] "Military standard MIL-STD 883 H," USA Department of Defense Std. method 3015.8, 2010.

[11] "Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components (JESD22-C101C)," JEDEC, 2004.

[12] J. Liou, Electrostatic Discharge Protection: Advances and Applications, Taylor and Francis Group, 2016.

[13] M. Ker and S. Hsu, "Component-Level Measurement for Transient-Induced Latch-up in CMOS ICs under System-Level ESD Considerations," *IEEE Transaction on Device and Material Reliability*, vol. 6, no. 3, pp. 461-472, 2006.

[14] M. Elghazali, M. Sachdev and A. Opal, "A Low-Leakage, Robust ESD Clamp with Thyristor Delay Element in 65 nm CMOS Technology," in *IEEE Computer Society Annual Symposium on VLSI*, 2016.