Electrostatic Discharge: A Reliability Threat to Integrated Circuits

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***Abstract*—CMOS integrated circuits are ubiquitous. Today's MOS transistors have gate insulator thickness of 1 nm and channel lengths approaching 10 nm. Despite the best efforts of factory ESD specialists and product design engineers to reduce the amplitude of the ESD currents that may reach an IC, the nanoscale transistor dimensions make it challenging to ensure that the current densities and induced electric fields remain below levels at which physical damage occurs. On-chip ESD protection circuits are a requirement for CMOS ICs. In essence, the ESD phenomenon provides job security for IC reliability engineers.**

This presentation will review the variety of ESD-induced hard and soft failures found in ICs. An introductory-level survey of on-chip ESD protection circuits will be provided.